Contents

FEATURES 4
GENERAL DESCRIPTION 4
1. ORDERING INFORMATION 6
2. BLOCK DIAGRAM 7
3. CONNECTION DIAGRAMS 8
4. SIGNAL DESCRIPTIONS 9
4.1. Serial Data Input (DI) / IO0 9
4.2. Serial Data Output (DO) / IO1 9
4.3. Serial Clock (CLK) 9
4.4. Chip Select (CS#) 9
4.5. Write Protect (WP#) / IO2 10
4.6. HOLD (HOLD#) / IO3 10
4.7. RESET (RESET#) / IO3 10
5. MEMORY ORGANIZATION 11
5.1. Flash Memory Array 11
5.2. Security Registers 11
5.2.1 Security Register 0 12
5.2.2 Serial Flash Discoverable Parameters (SFDP) Address Map 12
5.2.3 SFDP Header Field Definitions 13
5.2.4 JEDEC SFDP Basic SPI Flash Parameter 14
6. FUNCTION DESCRIPTION 19
6.1 SPI Operations 19
6.1.1 SPI Modes 19
6.1.2 Dual SPI Modes 19
6.1.3 Quad SPI Modes 19
6.1.4 QPI Function 20
6.1.5 Hold Function 20
6.1.6 Software Reset & Hardware R Tm [(.....)] TJ ET EMC /P.....89 379.26 2

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The ZB25VQ32 support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (WP#), and I/O3 (HOLD# / RESET#). SPI clock frequencies of up to 120MHz are supported allowing equivalent clock rates of 240MHz (120MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

The ZB25VQ32 provides an ideal storage solution for systems with limited space, signal connections, and power. These memories' flexibility and performance is better than ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

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1. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

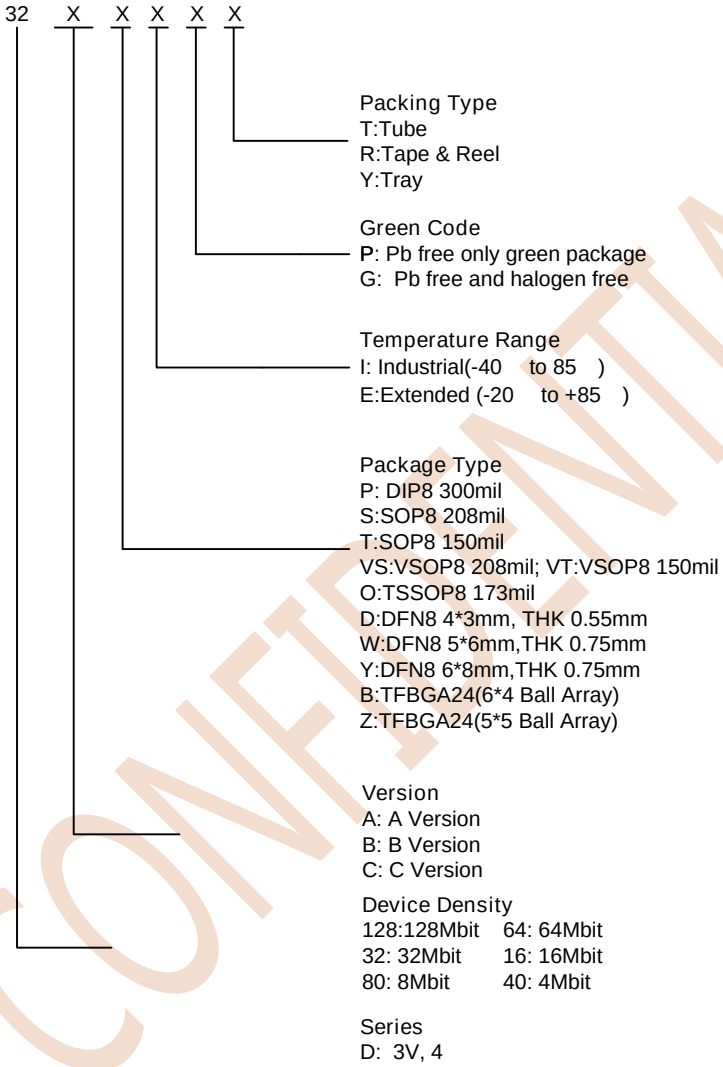

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Figure 1.1 Ordering Information

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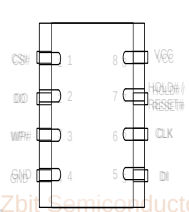

Figure 3.1 SOP8 (150/208mil)/ DIP8 (300mil)

Figure 3.2 DFN8 (5*6 mm)

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5.2.1 Security Register 0

Serial Fla sh Discoverable Parameters (SFDP ² JEDEC JESD216B):

This document defines the Serial Flash Discoverable Parameters (SFDP) revision B data structure for ZB25VQ32 family.

The Read SFDP (RSFDP) command (5Ah) reads information from a separate flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216B standard for Serial Flash Discoverable Parameters.

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instructions, the DI and DO pins become bidirectional IO0 and IO1, and the WP# and HOLD# / RESET# pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 QPI Function

The ZB25VQ32 supports Quad Peripheral Interface (QPI) operations when the device is switched from 6WDQGDUG 'XDO 4XDG 63, PRGH WR 43, PRGH XVLQJ a typical SPI protocol. QPI mode requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at DQ\ JLYHQ WLPH K \FY€@ W

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Table 7.3 Command Set (Read ID, OTP Instructions (1), SPI Mode)

Command Name	BYTE 1 (Instruc tion)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Deep Power-down	B9h					
Release Power down / Device ID	ABh	dummy	dummy	dummy	Device ID(1)	
Manufacturer/ Device ID(2)	90h	dummy	dummy	00h	Manufacturer	Device ID
Manufacturer/ Device ID by Dual I/O	92h	A23 ² A8	A7 ² A0,M[7:0]	(MF[7:0],ID[7:0])		
Manufacturer/ Device ID by Quad I/O	94h	A23 ² A0,M[7:0]	XXXX,(MF[7:0],ID[7:0])	(MF[7:0],ID[7:0]...)		
JEDEC ID	9Fh	Manufacturer	Memory Type	Capacity		
Read SFDP Register	5Ah	00h	00h	[redacted]		

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7.3 Read Commands

7.3.1 Read Data (03h)

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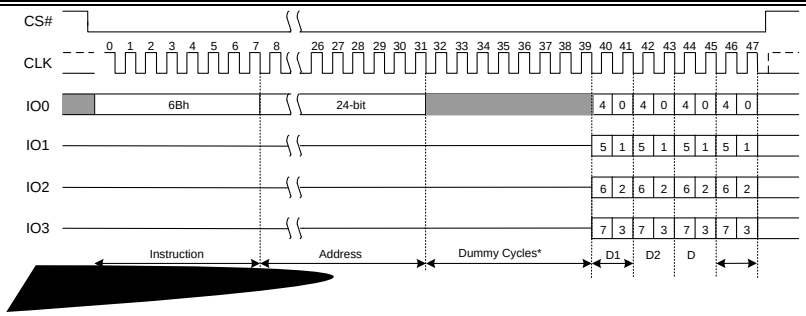

Figure 7.16 Fast Read Quad Output Instruction

7.3.5 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per dock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7.17. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("X"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

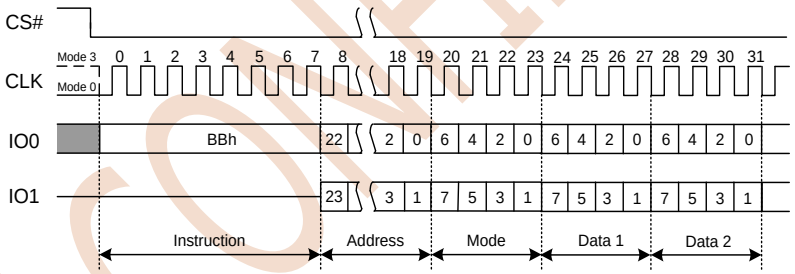

Figure 7.17 Fast Read Dual I/O Instruction (Initial command or previous M5- •

Note:
/HDVW VLJQLILFDQW ELWV RI 0RGH DUH GRQ¶W FDUH DQG LW LV RSWLRQDO IRU WKH
Drive during these cycles to increase bus turnaround time between Mode bits from host and returning data from the memory

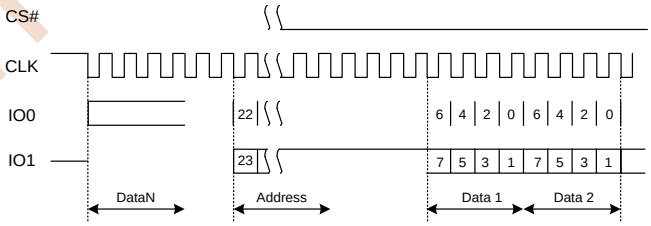

Figure 7.18 Fast Read Dual I/O Instruction (Initial command or previous M5-4=10)

7.3.6 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and Dummy clock are

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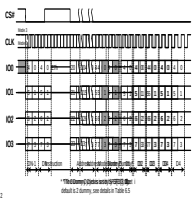
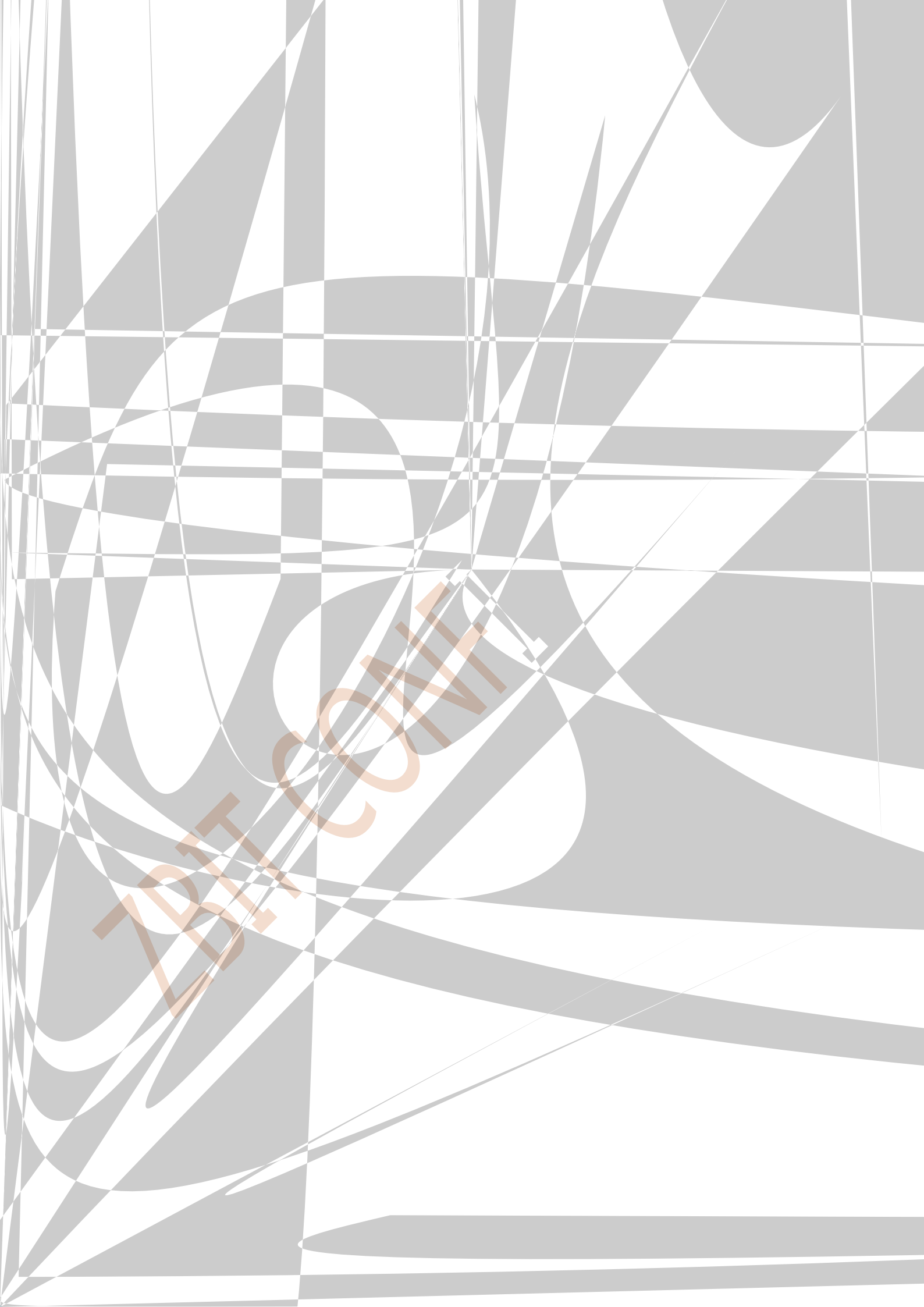


* This is Extended Dummy Cycles setting by SPI/QPI/DTR command
Default is 2 dummy, see details in Table 6.5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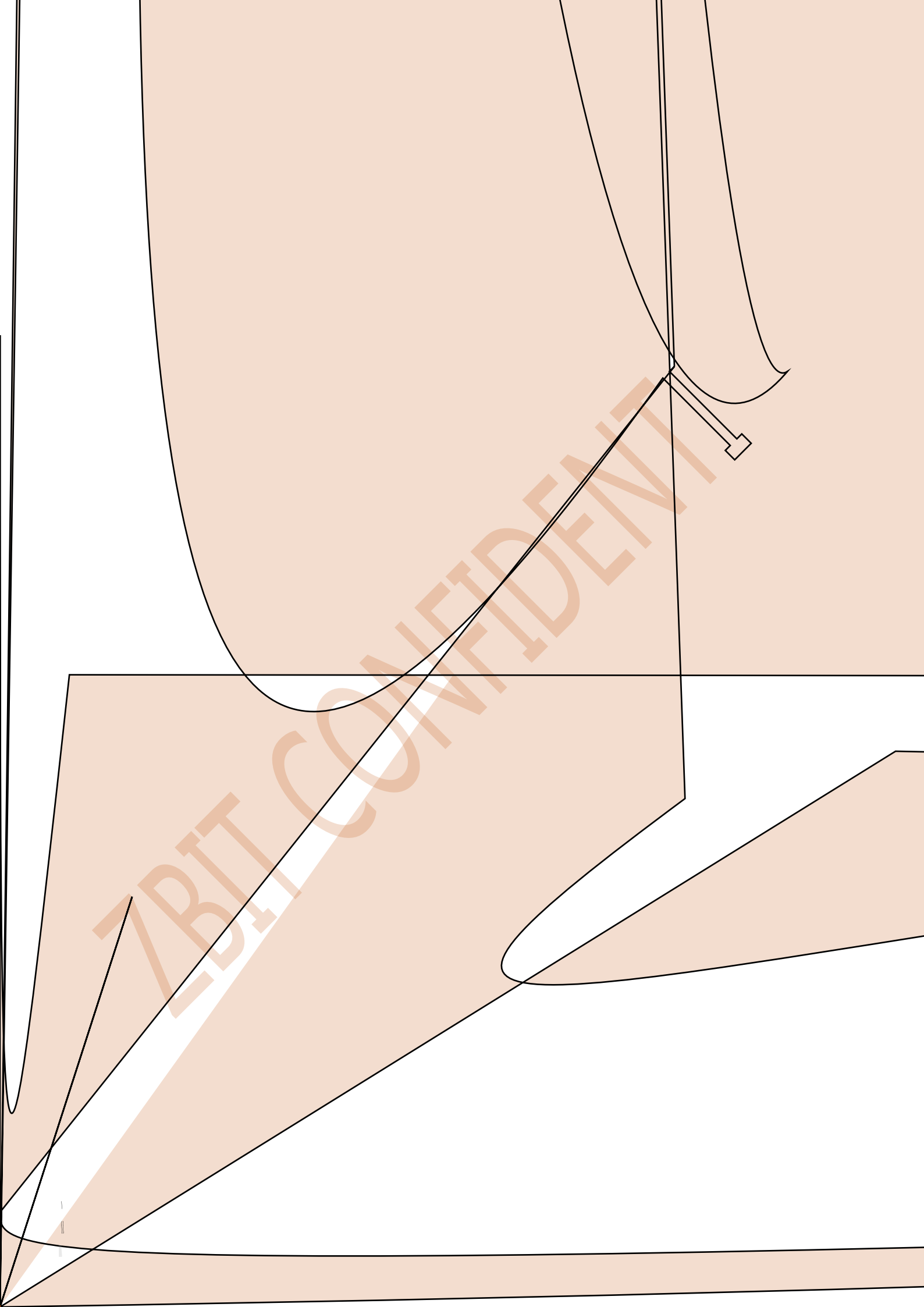
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speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruc W L R Q F R G H ³ K´ I R O O R Z 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.36. The Device ID values for the ZB25VQ32 are listed in Table 8.1. The Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

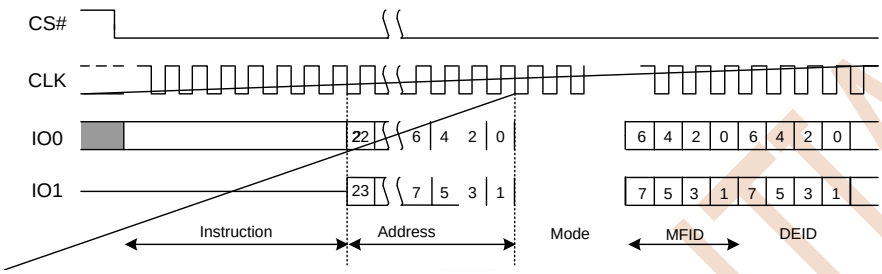

Figure 7.36 Read Manufacturer/Device ID Dual I/O Instruction

Note:

1. The "Continuous Read Mode" bits M7-0 must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

7.5.10 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4 x speeds.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "94h" followed by a 24-bit address(A23-A0) of 000003 ET c".BT 1 0 0 1 214.13 542.23 Tm 0 Tc[(Re)-1027.59 ( )25(00)4(0,3(s)-5(()8BT 1 0 0

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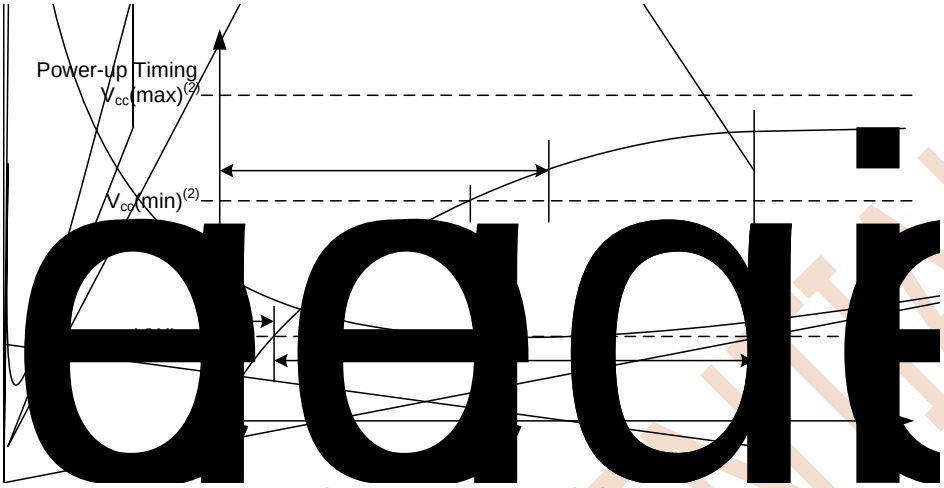

Figure 8.1 Power-up Timing

Table 8.1 Power-up Timing

PARAMETER	SYMBOL	TYPE		UNIT
		MIN	MAX	
Vcc(minimum operation voltage)	Vcc(min)	2.3	-	V

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8.1. Absolute Maximum Ratings

Stresses above the values mentioned as following may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values.

Table 8.2(1) Absolute Maximum Rating

PARAMETERS(2)	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	V_{CC}		-0.6 to +4.0	V
Voltage applied on any pin	V_{IO}	Relative to Ground	-0.6 to V_{CC}+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-2.0 to V_{CC}+2.0	V
Storage Temperature	T_{STG}		-65 to +150	-
Lead Temperature	T_{LEAD}			

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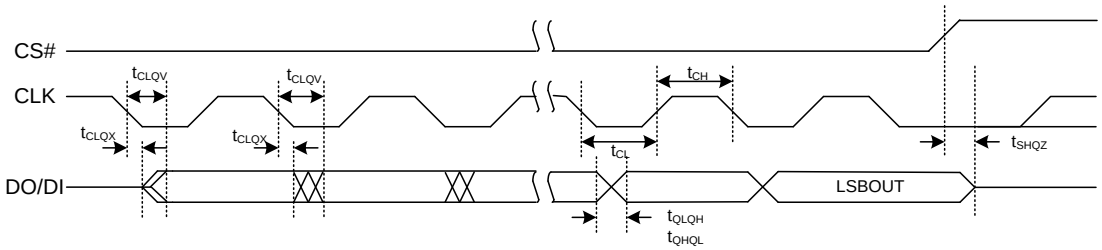

*DIO IS AN OUTPUT ONLY FOR THE FAST READ DUAL OUTPUT INSTRUCTIONS (3BH)

Figure 8.4 Serial Output Timing

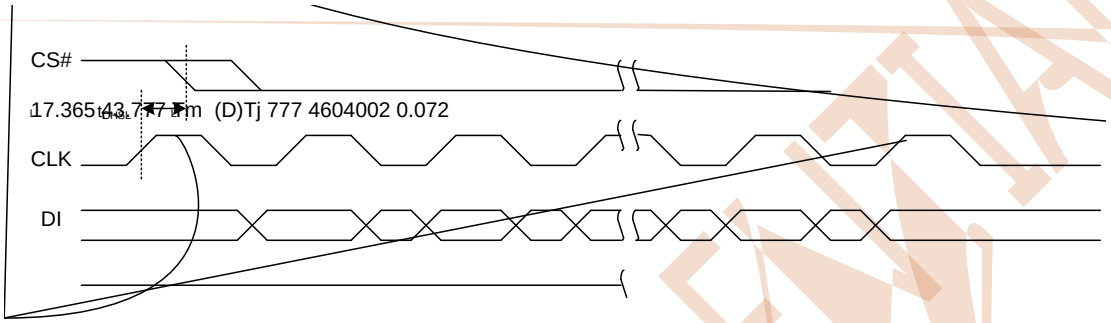

Figure 8.5 Input Timing

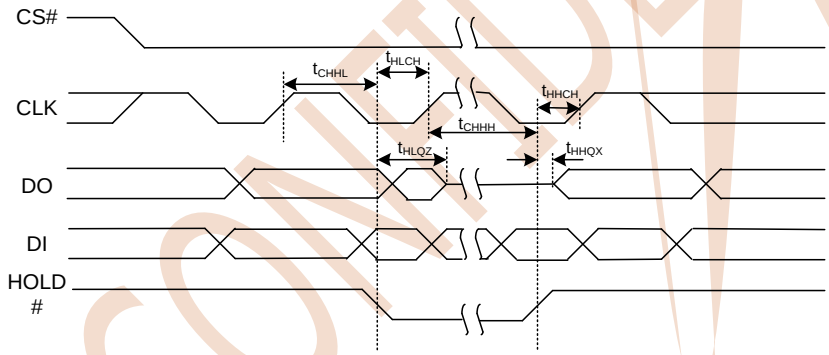

Figure 8.6 Hold Timing

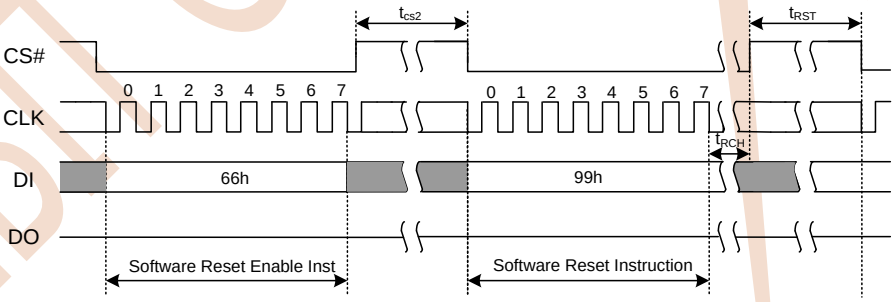

Figure 8.7 Software Reset Input Timing

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